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# A low-resolution vision sensor

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**Abstract.** A low-resolution camera system based on a 64k dynamic RAM chip is described. The camera is capable of providing a picture resolution of up to 256 × 128 pixels. A fast microprocessor is used to collect the picture data and to provide a preprocessing facility and a flexible means of access to the data.

## 1. Introduction

This paper describes a camera system of low resolution (up to 256 × 128 pixels) which is eminently suitable for such purposes as component inspection and identification. The use of a low-cost dynamic RAM chip as a light sensor provides a method of imaging not really obtainable by any other means. Area CCD cameras (as distinct from line-scan arrays), such as the Sony XC-37 and Fairchild CCD3000, though providing a greater resolution, are an order of magnitude greater in cost: ranging from £700 to some £2000. These types of camera are not strictly comparable with a dynamic RAM camera as they give grey scale imaging directly and are designed to be compatible with television displays. As such, imaging data is not as easily obtainable from them in a form suitable for input to a microcomputer system. Also, the larger resolution of the CCD camera is not always necessary for parts inspection and identification. In such cases, a RAM camera system, costing only around £100 to build, can be a more appropriate instrument.

Details are given in the paper of the circuits used to interface to the camera, and the visual data is obtained in a form convenient for capture and subsequent processing by a microcomputer system.

## 2. The camera

### *2.1. Construction*

The camera is a simple structure using as the light-sensitive element a dynamic RAM chip specifically constructed for optical work: the silicon chip is housed within a ceramic package with a built-in window to allow light to be focused onto the active part of the silicon. This device, the IS32, is a development of the μT4264 64k DRAM (Micron Technology Inc.) and is currently priced at £33. A small projector-type lens (focal length 9 mm) is used to focus the image, figure 1. The lens is threaded, allowing focal adjustment. This is not critical, the effect of exposure time and focus being rather similar in that memory cells on the fringe of images may or not be affected depending on either the sharpness of the image or the sensitivity of the array. In practice we have found that a combination of 'coarse' focal length and a lens stop can be chosen to suit the application and 'fine tuning' effected by means of the exposure time. It should be noted that, unlike, say, a Vidicon tube, over-exposure has no detrimental effect on the RAM chip.

The camera body is constructed from black 'nylatron' plastic and connection to the drive electronics is via 16-way ribbon cable. The overall size of the camera is 2.5 × 2 × 3 cm.

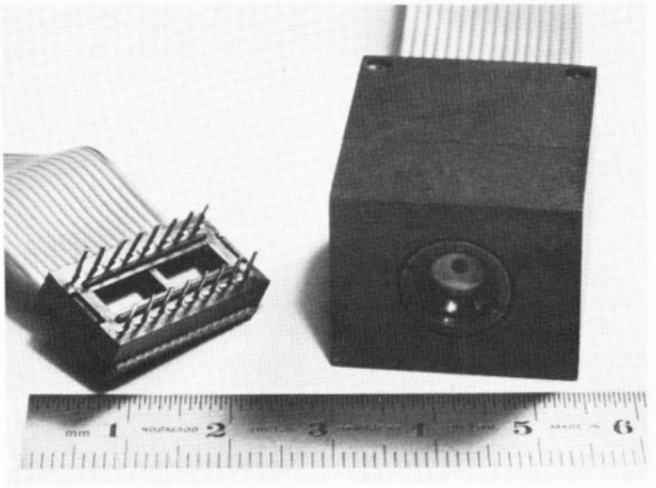

**Figure 1.** The camera unit.

### *2.2. The light-sensitive array*

The IS32 is a 64 × 1 bit dynamic RAM chip laid out as two 32k bit arrays, physically separated by the sense amplifiers. As a consequence of this, only one half of the available RAM can conveniently be used for the picture array.

Data is held in a DRAM by charge storage. In 'normal' use, this charge would gradually leak away due to thermal effects and the information be lost were it not that the charge is replenished by 'refresh' circuitry built into the chip which replaces the charge automatically upon row selection during the reading process. It is therefore necessary to ensure that the entire array of a DRAM is read at regular intervals so that refreshing may take place. In microcomputer systems dynamic RAM refresh takes place automatically and is transparent to the user.

As well as thermal effects, photoelectric current will discharge the data cells and it is this photoelectric effect that is exploited to provide a light-sensitive array. By precharging the memory cells and reading their state at regular intervals a representation of light incidence on the array can be obtained in terms of 'ones' and 'noughts' (Russell 1983). The image obtained by this process is binary in nature, the amplifiers within the DRAM interpreting any level of charge as one of the two logic levels. It is possible to produce a grey scale image but this must be done by taking repeated 'snap shots' at different exposure times and then processing the resulting set of images into a single composite picture.

Our initial experiments on the use of commercially available DRAM devices as low-resolution camera elements centred upon the 4116 DRAM. Earlier versions of this device were housed in a ceramic package with a metal lid which could be removed (carefully) and replaced by a thin piece of glass (Hodgson 1982). A disadvantage of the 4116 concerns its topology – the storage cells are not arranged in straight rows, rather in a diagonal manner. This gives a castellated edge effect to images. Note that a commercial camera (type 511 Image Digitizer, Periphicon Inc.) uses a DRAM chip similar to the now obsolete MK4006 DRAM (Mostek Inc.). This chip does not have on-board refresh circuitry (an advantage for imaging work) but the array size restricts resolution to 32 × 32 pixels. The IS32 by comparison has its cells organised in straight rows and is therefore more suitable for camera work. It should be noted that the separation of each cell on the IS32 is not equal: the row/column bit spacing is 21.5 μm/8.5 μm. This means that images are distorted when

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viewed with a direct mapping from the DRAM to a VDU screen. For computer analysis, this is unimportant and in some instances can be used to advantage. For example, only circular objects will present a constant area (equal number of pixels) when presented to the camera and then rotated.

### 2.3. Exposure time

In use, a 'read-modify-write' cycle is employed: addressed cells are charged by a write cycle immediately after being read. Note that the internal arrangement of the cells demands that for half of the array logical 'one' corresponds to a charged cell and for the other half logical 'nought' indicates the presence of charge. Connecting the most significant address bit to $D_{in}$, figure 3, takes care of this inversion. The read cycle time relates to the 'exposure' time directly. The automatic refresh that takes place during each row selection has the effect of 'setting' the charge level in the cells to either the 'one' or the 'nought' level. Thus the effective exposure time is the time between each row selection. For a continuously running clock, the exposure time is given by:

$$t_{exp} = (N_R - 1) \cdot N_c \cdot t$$

where

$N_R$ = number of rows

$N_C$ = number of columns

$t$ = system clock period.

In the present design, $t$ can be varied between one and six microseconds, giving a wide range of exposure times.

## 3. Hardware

To obtain correct exposure times under normal lighting levels it was found that a clock rate of approximately 0.8 MHz was necessary for the DRAM. At this rate, transfer of data from the IS32 to a RAM store presents several problems. Either discrete logic must be used to manipulate the data, or a fast microprocessor is required. The latter approach was chosen as it seemed to offer a greater degree of flexibility for subsequent work.

A block diagram of the microprocessor system is shown in figure 2 and the IS32 drive circuitry is shown in figure 3. The camera is controlled by an Intel 8031 microprocessor. This device can operate at clock speeds up to 12 MHz. The camera clock is derived from the processor clock and through the 74LS393 counters, (figure 3), generates the memory addresses for the IS32. The exclusive-OR gates are required to 'unscramble' the IS32 addresses since the physical positions of the cells on the chip do not correspond to their logical positions. Serial data from the DRAM are converted into 8-bit parallel data bytes by the 74LS164 shift register, clocked into the 74LS374 8-bit latch,

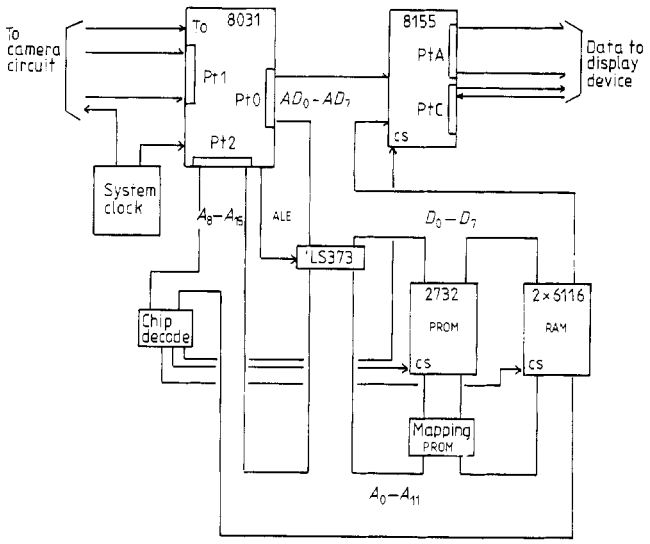



**Figure 2.** The 8031 microprocessor control system.

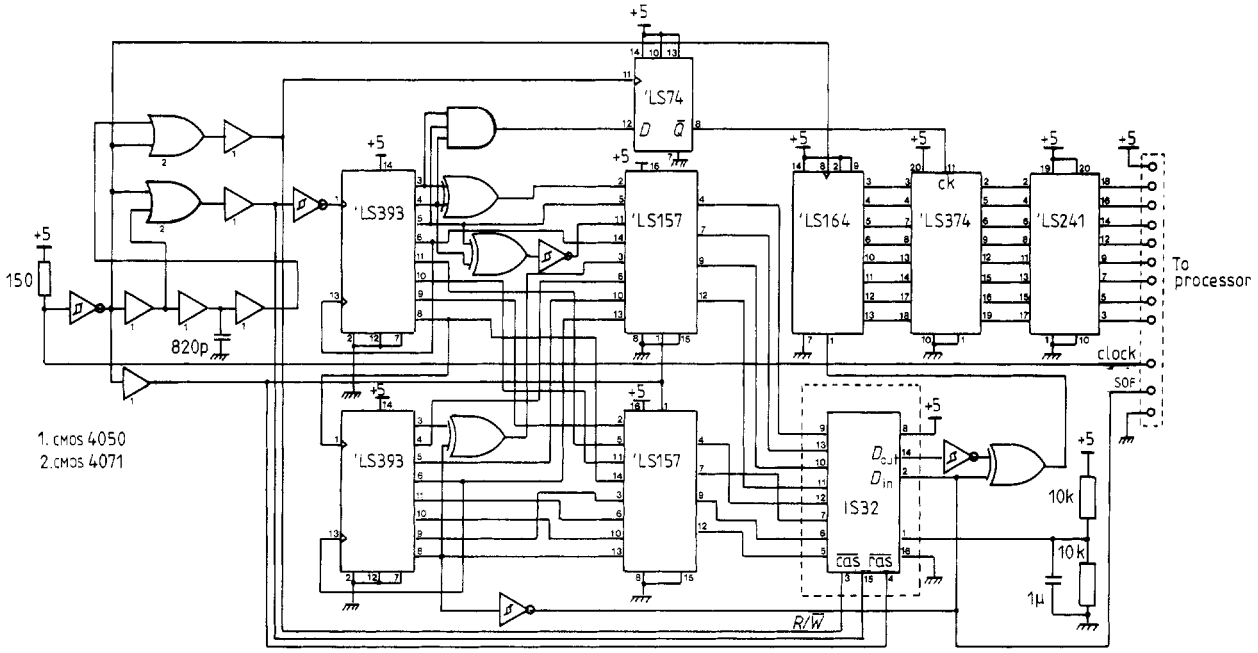



**Figure 3.** The camera drive electronics.

**Table 1.** Data capture program for the 8031.

```
READ:       NOP             ;Waste some time.
            MOV A, P1       ;Read in data byte from IS32.
            MOVX DPTR, A    ;Store video data in RAM.
            INC DPTR        ;Point to next free location.
            ORL ACC, $OOH   ;Waste more time here.
READ LOC:                   ;Entry point to recurrent 8 byte.
                            ;image stream.
```

and then, through the 8-bit driver, 74LS241, transmitted via ribbon cable to the processor.

By using a clock signal for the IS32 which is derived from the 8031 clock circuits, a software–hardware synchronous system is created. A 'handshake' is then not necessary for the transfer of data to the 8031 from the camera, a 'start-of-frame' (SOF) being all that is required. The 8031 program shown in table 1 is timed to synchronise with the data byte rate from the shift register. This program stores an IS32 picture byte into a given location in the fast 6116 RAM used as the picture store. By modifying the address decode to the PROM containing this short program it is possible to force the 8031 to repeat this code 4k-1 times, thus enabling a complete picture frame to be stored as 8-bit bytes in successive locations in the RAM. After the 4k iterations of this program section the 8031 'falls through' and accesses the next section. Figure 4 gives details of the PROM decode.

The SOF signal ensures correct synchronisation of the data capture sequence. Since that data is present for at least eight microseconds, sufficient time is available to branch into the capture sequence following the SOF signal. Note that this SOF signal, derived from the IS32 address, provides a positive-going edge at the commencement of addressing the first 32k block of the IS32 DRAM and a negative-going edge when the second block is addressed. By altering the polarity of the edge detector, either half of the IS32 may be selected. When a complete frame from the IS32 (32k bits) has been captured, the 8031 can be used to process the data. In our present system, only limited modification is made before outputting the data to a display system (Motorola Exorset). The processing carried out on the pictures shown (figures 5(*a*)–(*c*)) was simply to reduce the amount of data by masking out the odd-addressed bits and then duplicating the even ones. This maintains a 4k byte frame but reduces considerably the picture noise. This noise appears to be caused by a 'nearest neighbour' disturbance effect or simply the result of light fringing. The effect is to produce a chequered pattern of pixels at light/dark boundaries. Selecting alternate pixels removes this but with the penalty of a reduction in resolution to 64 × 128 pixels. The pictures show that even with this small amount of processing, excellent results can be obtained.

The Motorola Exorset accepts the data as 8-bit bytes from the 8031 through its standard 6821 port interface and is used simply as a convenient medium for display and experimental processing of the images.

## 4. Conclusions

A simple low-cost camera system for use in inspection and parts identification work has been described. Good-quality picture resolution of 64 × 128 pixels can readily be obtained from a 128 × 256 pixel base. Details of an image processor for the video data have been given but the camera is suitable for use with most computer systems having an interface capable of accepting serial data at a one megahertz bit rate. The use of the Exorset

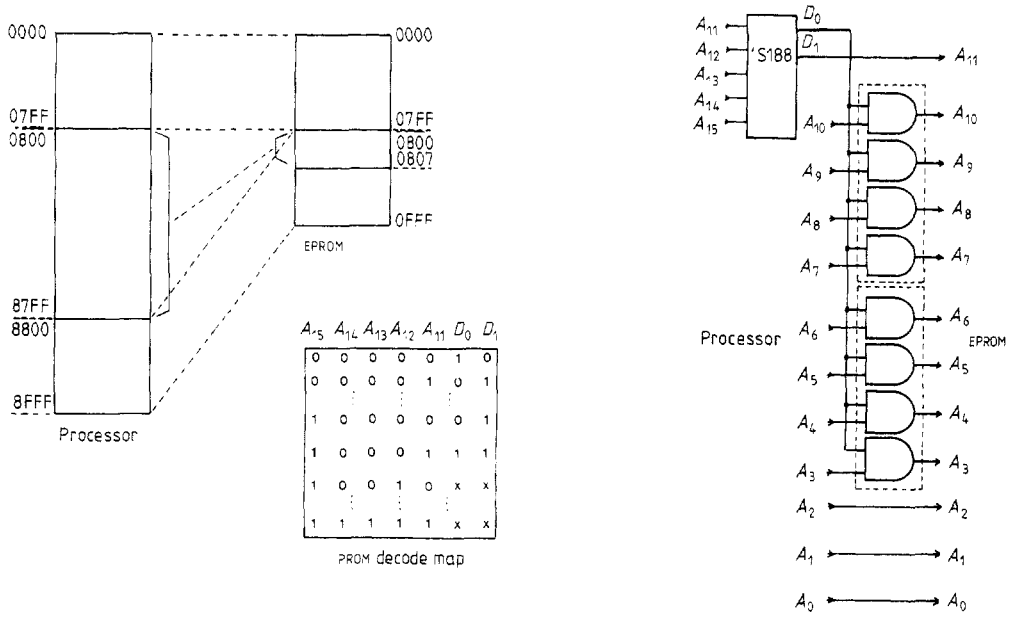
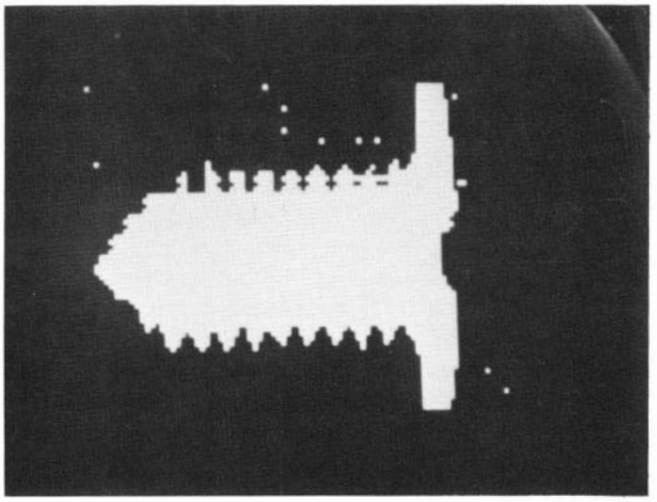
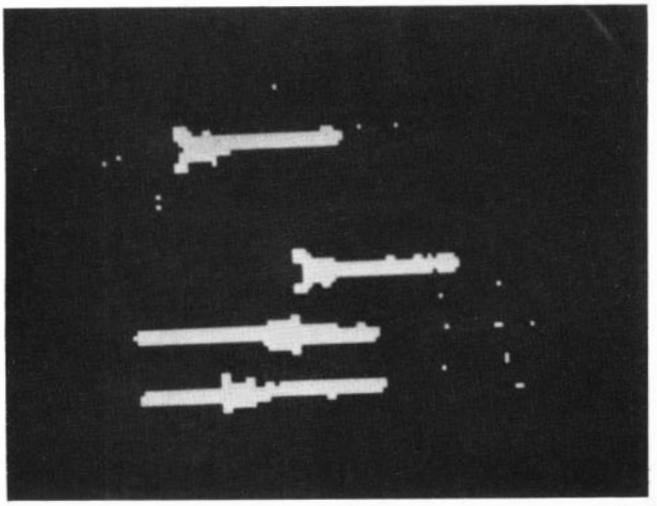


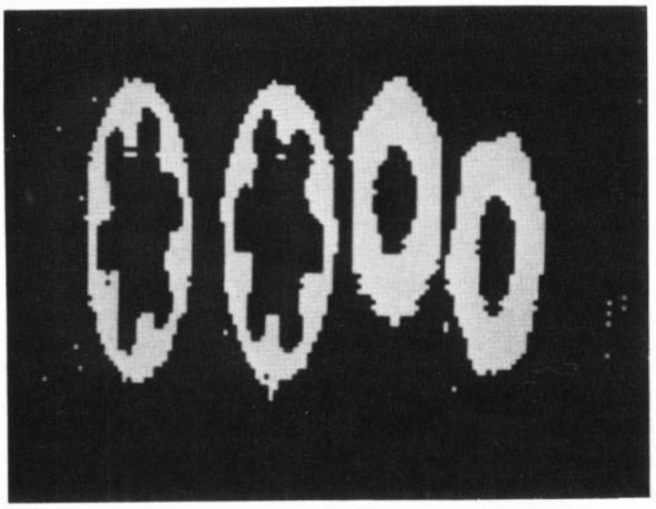

**Figure 4.** PROM decode and mapping.



(a)



(b)



(c)

**Figure 5.** (*a*), A self-tapping screw; (*b*), single- and double-sided PCB pins; (*c*), shake-proof and circular washers. Note the distortion caused by the unequal aspect ratio of the pixel spacing.

has been found to be most convenient for our image-processing development work; in particular recognition of edges, beacons, and the calculation of centroids. Such facilities will eventually be transferred to the 8031 which will then function as an 'intelligent' slave processor in the multiprocessor system (Mitchell *et al* 1983) at present under development within the Department for use in the investigation of robot assembly tasks.

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